REMARKS

The present application was filed on August 13, 1999 with claims 1-18. Claims 1 and 15-18 are the independent claims.

In the Office Action, the Examiner rejected claims 1-11, 15 and 16 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,418,176 (hereinafter "Ho"), rejected claims 17 and 18 under §102(e) as being anticipated by U.S. Patent No. 6,249,542 (hereinafter "Kohli"), and indicated that claims 12-14 contain allowable subject matter.

In this response, Applicants amend independent claim 17, and traverse the §102(e) rejections. Applicants respectfully request reconsideration of the present application in view of the following remarks.

Applicants initially note that the Manual of Patent Examining Procedure (MPEP), Eight Edition, August 2001, §2131, specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). For the reasons identified below, Applicants submit that the Examiner has failed to establish anticipation of at least independent claims 1 and 15-18.

With regard to independent claim 1, this claim calls for a logic circuit and a selection circuit. The logic circuit is coupled to outputs of each of first, second and third processing circuits, and operative to generate a control signal indicative of the presence or absence of a desired relationship between at least one clock signal and first, second and third versions of a given signal. The selection circuit has an input coupled to an output of the logic circuit, and is responsive to the control signal to alter a relationship between the clock signal and the first, second and third versions of the given signal if the control signal indicates the absence of the desired relationship.

The Examiner argues that these limitations are met by the Ho reference. Applicants respectfully disagree. In formulating the §102(e) rejection over Ho, the Examiner states that the claimed first, second and third processing circuits correspond to flip-flops 92, 94 and 96,

respectively, of the FIG. 5 circuit in Ho. The Examiner further states that the claimed logic circuit corresponds to multiplexers 100, 102 of FIG. 5, and that the claimed selection circuit corresponds to multiplexers 70, 72 of FIG. 5. However, even if one assumes that this alleged correspondence between circuit elements of claim 1 and elements of Ho FIG. 5 is correct, the FIG. 5 circuit nonetheless fails to meet the particular claim limitations outlined above. As indicated above, claim 1 specifies that the selection circuit is responsive to the control signal generated by the logic circuit to alter a relationship between the clock signal and the first, second and third versions of the given signal if the control signal indicates the absence of the desired relationship.

In FIG. 5 of Ho, the outputs J and K of the multiplexers 100, 102, which the Examiner has characterized as the claimed logic circuit, are supplied as inputs to the respective multiplexers 70 and 72, but the multiplexers 70, 72, which the Examiner has characterized as the claimed selection circuit, are not responsive to either of the J or K signals to alter a relationship as claimed. Instead, the selection states of the multiplexers 70, 72 are controlled by respective MUX3 and MUX4 signals generated by the control circuit 86 in FIG. 3 of Ho, which does not itself receive as inputs the J, K signals generated by multiplexers 100, 102. This is also apparent from column 6, lines 47-49 of Ho, wherein it is stated that "[t]he control circuit 86 operates the output multiplexers 70, 72, 74, 76 such that the data is read from the FIFO circuit 66, 68, and provided to the output flip-flops 78, 80, 82, 84 in two consecutive cycles of the recovery clock signal." Therefore, the multiplexers 70, 72 are not responsive to a control signal from the multiplexers 100, 102 in the particular manner claimed, and claim 1 is thus not anticipated by Ho in the manner alleged by the Examiner.

Dependent claims 2-14 are believed allowable for at least the reasons identified above with regard to their corresponding independent claim 1. Moreover, one or more of these claims are believed to define separately-patentable subject matter relative to Ho, Kohli and the other art of record.

Independent claim 15 includes logic circuit and selection circuit limitations similar to those of claim 1, and is therefore believed allowable for at least the reasons identified above with regard to claim 1.

Independent claim 16 calls for generating a control signal indicative of the presence or absence of a desired relationship between at least one clock signal and first, second and third

versions of a given signal, and altering a relationship between the clock signal and the first, second and third versions of the given signal if the control signal indicates the absence of the desired relationship. Again, the Examiner characterizes the claimed control signal as corresponding to the J or K output of the multiplexers 70, 72 in FIG. 5 of Ho. However, the J or K outputs of the multiplexers 70, 72 are not utilized to alter a relationship in the particular manner claimed. It should also be noted that the control circuit 86 does not alter a relationship between a clock signal and first, second and third versions of a given signal if the control signal indicates the absence of a desired relationship.

Independent claim 17 as amended calls for a feedback control circuit having an input coupled to outputs of each of first, second and third processing circuits, and operative: (i) to generate a control signal indicative of the presence or absence of a desired phase relationship between a second signal and first, second and third versions of a given signal, and (ii) to alter a phase relationship between the second signal and the first, second and third versions of the given signal if the control signal indicates the absence of the desired phase relationship. The Examiner argues that such an arrangement is shown in FIGS. 2, 3 and 4 of Kohli, and more particularly that the claimed control signal corresponds to the output of the current position element 70 of Kohli FIG. 2. Applicants respectfully disagree. The current position element 70 does not generate a control signal which meets the particular limitations (i) and (ii) noted above.

Independent claim 18 calls for a feedback control circuit having an input coupled to outputs of each of first, second and third processing circuits, wherein the feedback control circuit is operative to maintain a desired relationship between a second signal and first, second and third versions of a given signal based on sample values generated at the outputs of the first, second and third processing circuits. The Examiner argues that such a feedback control circuit is shown in Kohli. Applicants respectfully disagree. Applicants note that the Examiner has not identified with particularity the precise signals in Kohli which are alleged to correspond to the claimed given and second signals. In addition, the SAT processor 46 in FIG. 2 of Kohli does not have "an input coupled to outputs of each of first, second and third processing circuits." Instead, the SAT processor 46 receives results of a thresholding test performed by threshold test element 82. See Kohli at column 13, lines 12-21.

Also, the SAT processor 46 is not operative to maintain a desired relationship between a second signal and first, second and third versions of a given signal based on sample values as claimed.

In view of the above, Applicants believe that claims 1-18 are in condition for allowance, and respectfully request withdrawal of the §102(e) rejections.

A marked-up version of the changes made to the claims is attached hereto.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

17. (Amended) An apparatus comprising:

first, second and third processing circuits, each operative to perform a sampling function on a corresponding one of a first version, a second version and a third version of a given signal, the processing circuits performing the sampling function utilizing a second signal to which the given signal is to be synchronized; and

a feedback control circuit having an input coupled to outputs of each of the first, second and third processing circuits, and operative: (i) to generate a control signal indicative of the presence or absence of a desired phase relationship between the second signal and the first, second and third versions of the given signal, and (ii) to alter a phase relationship between the [at least one clock] second signal and the first, second and third versions of the given signal if the control signal indicates the absence of the desired phase relationship.